~~P4~~ Dataplane Programming and ~~GÉANT~~ (GLOBAL) P4 Lab (aka GP4L)

Frédéric Loui (RENATER)

10th SIG-NOC meeting

November 29 2022

On-line event

www.geant.org

Agenda

- RARE/**freeRtr** in a nutshell
- ~~**P4**~~Dataplane Programming
- A simple use case with RARE **P4** program

Router for Academia, Research and Education (RARE)

RARE is an open source routing platform, used to create a network operating system (NOS) on commodity hardware (a white box switch).

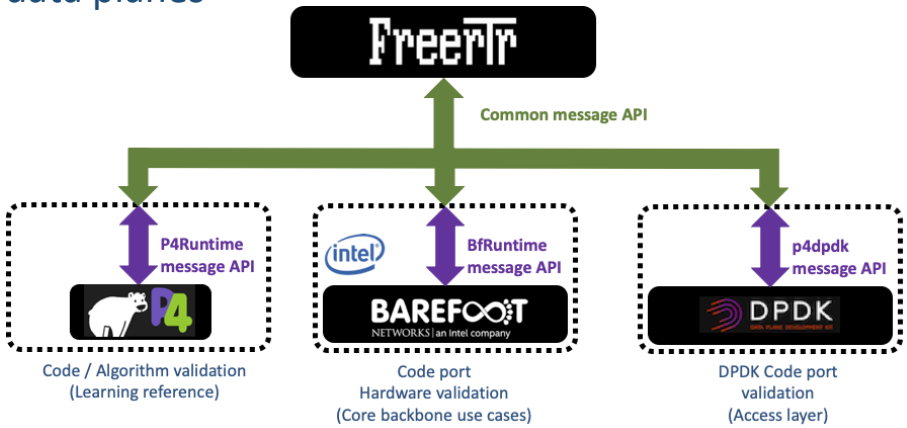
RARE uses FreeRtr as a control plane software and is thus often referred to as RARE/FreeRtr

FreeRtr

More information:
https://wiki.geant.org/display/rare

RARE/FreeRtr Basics

- Free and open source routing platform
- Controls the data plane by managing entries in Match Action Unit (MAU) tables
- Every routed interface must be in a virtual routing table, every layer interface in a bridge table
- One control, several data planes
- Exports control plane computation results to DPDK or hardware switches
- Uses Data Plane Programming (DPP) Language such as **P**rogramming **P**rotocol-independent **P**acket **P**rocessors: **P4** language



Programming Protocol-independent Packet Processors: P4 language

Language for **programming the data plane** of network devices

- Define how packets are processed
- P4 program structure: header types, parser/deparser, match-action tables, user-defined metadata and intrinsic metadata

Domain-specific language designed to be implementable on a large variety of targets

- Programmable network interface cards, FPGAs, software switches and hardware ASICs

Programming Protocol-independent Packet Processors: P4 language

P4 Programmable Switches

EdgeCore Wedge100BF-32QS:

- 100GbE Data Center Switch
  - Bare-Metal Hardware
  - L2/L3 Switching
  - 32xQSFP28 Ports
- Data-Plane Programmability
  - Intel Tofino Switch Silicon
  - Barefoot Networks
- Quad-Pipe Programmable Packet Processing Pipeline
  - 6.4 Tbps Total Bandwidth
- CPU: Intelx86 Xeon 2.0GHz
  - 8-core/48GB/2TB SSD

TOFINO 2™
12.8 Tbps
32x400 GE ports

TOFINO 3™
25.6 Tbps
64x400 GE ports

TOFINO 1 ™
6.4 Tbps

P4 Programmable Switches

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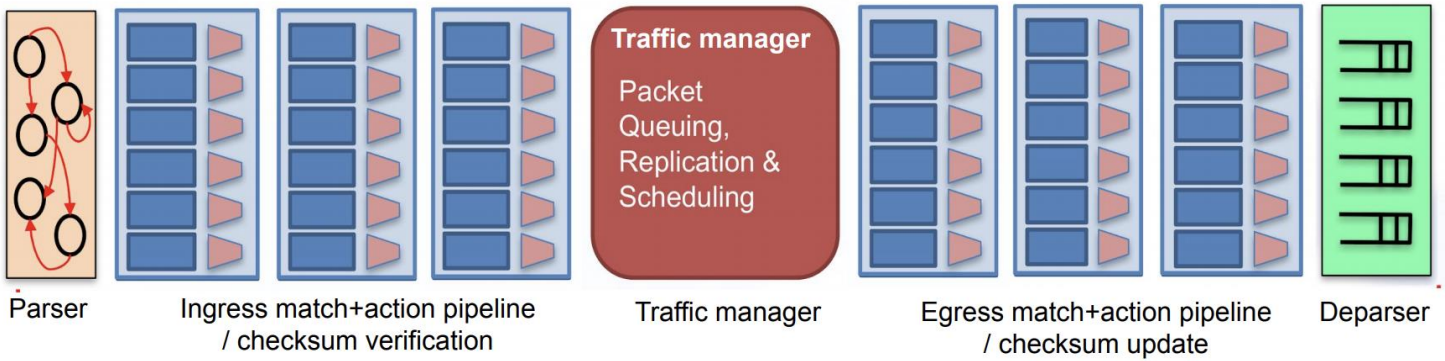
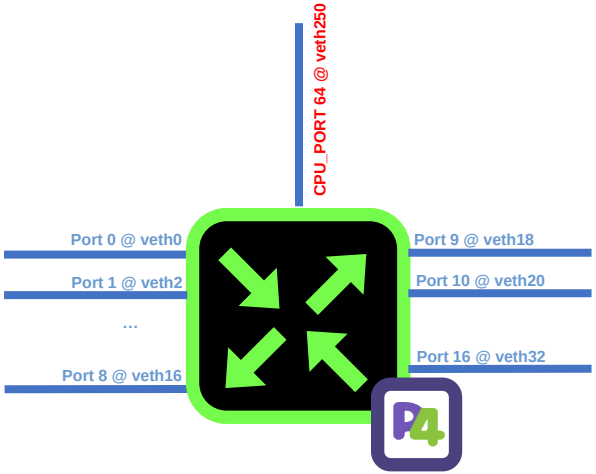
Portable Service Architecture (PSA) model



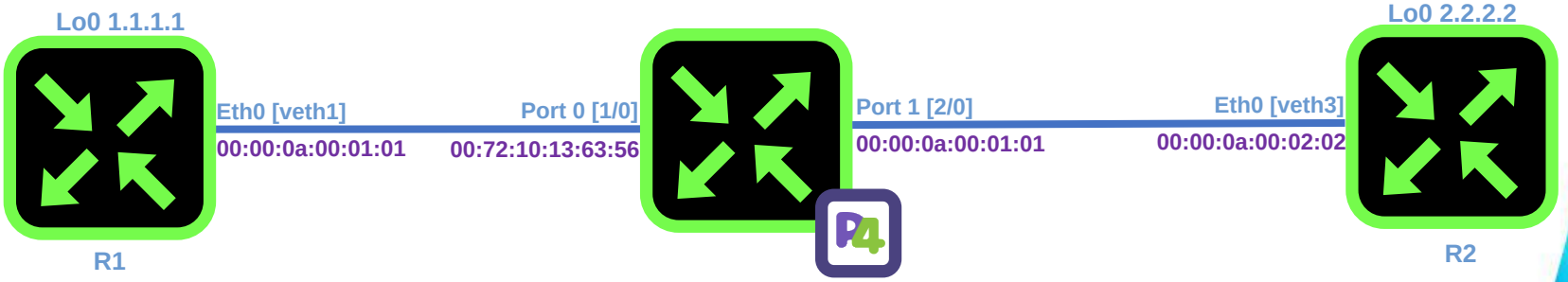
Slide courtesy P4.org

RARE P4 program (aka bf_router.p4) demo

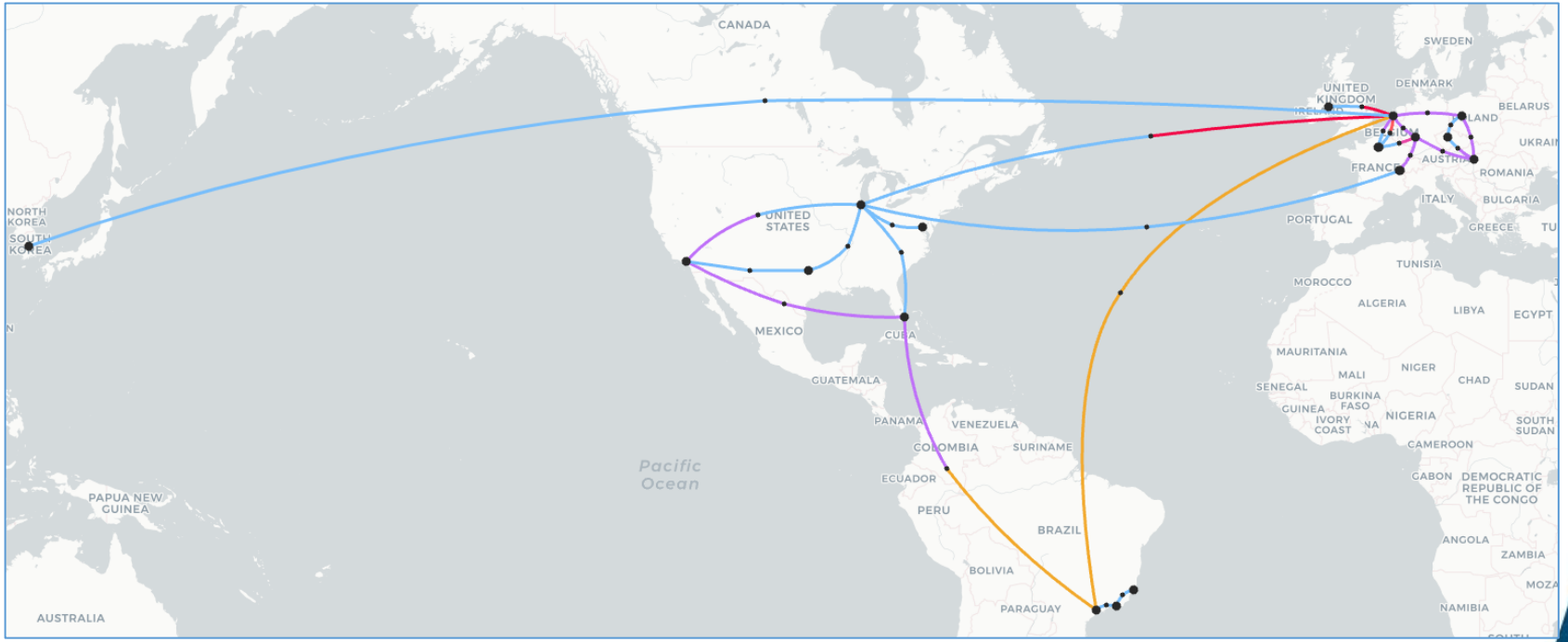
bf_switchd target virtual model



RARE bf_router.p4



GP4L November 2022 during SC22 !



Develop & test your P4 program with GP4L !

Looking ahead

Validate your use case with GP4L!

Orchestrate and automate GP4L:
Lab reservation
Persistent testbed interaction at global scale

New hardware:
TOFINO2, NVIDIA DPU, P4 SmartNIC, TOFINO/FPGA

Global worldwide footprint:
Interconnection with other persistent testbed

New idea:
Validate new use cases
Focus on use case scalability
100/400 GE DTN automation
Control plane scalability

And more …

Key take-away

- DPP is not only about **P4**
- **P4** is a DSL familiar to network engineer
- **GP4L** is available for R&E partner in order to validate P4 code
- **RARE** dataplane can be automated by your control-plane

Useful Links

Documentation:

GP4L project: https://wiki.geant.org/display/GP4L/

RARE/FreeRtr: https://wiki.geant.org/display/RARE
https://blog.freertr.org
https://docs.freertr.org
https://blog.freertr.org

GÉANT NETDEV: https://wiki.geant.org/display/NETDEV

Contact:

Users: gp4l-users@lists.geant.org, rare-users@lists.geant.org

Developers: gp4l-dev@lists.geant.org, rare-dev@lists.geant.org

Project: gp4l@lists.geant.org, rare@lists.geant.org

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Thank you

Any questions?

Email: ***netdev@lists.geant.org***

www.geant.org

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