

## RARE / freeRtr

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10th SIG-NOC meeting

November 29 2022

On-line event

www.geant.org



#### Agenda

- RARE/freeRtr in a nutshell
- One control plane to rule them all (Or vice versa)
- A simple use case with RARE P4 program
- POLKA: A GP4L use case



#### Router for Academia, Research and Education (RARE)

RARE is an open source routing platform, used to create a network operating system (NOS) on commodity hardware (a white box switch).



RARE uses FreeRtr as a control plane software and is thus often referred to as RARE/FreeRtr



More information:

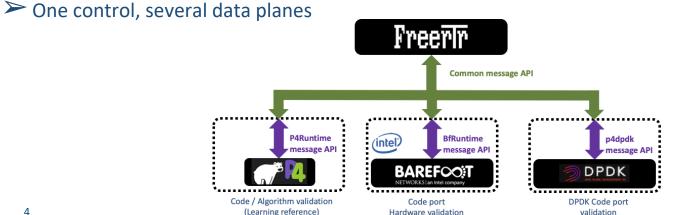
https://wiki.geant.org/display/rare

#### **RARE/FreeRtr Basics**

- Free and open source routing platform
- Controls the data plane by managing entries in Match Action Unit (MAU) tables
- Every routed interface must be in a virtual routing table, every layer interface in a bridge table

- Exports control plane computation results to DPDK or hardware switches.
- Uses Data Plane Programming (DPP) Language such as **Programming** Protocol-independent Packet Processors: P4 language

(Access layer)



(Core backbone use cases)



#### **Programming Protocol-independent Packet Processors: P4 language**

Language for **programming the data plane** of network devices

- Define how packets are processed
- P4 program structure: header types, parser/deparser, match-action tables, userdefined metadata and intrinsic metadata

**Domain-specific language** designed to be implementable on a large variety of targets

Programmable network interface cards,
 FPGAs, software switches and hardware ASICs



## **Programming Protocol-independent Packet Processors: P4 language**





#### **P4 Programmable Switches**

#### **EdgeCore Wedge100BF-32QS:**

100GbE Data Center Switch

- Bare-Metal Hardware
- L2/L3 Switching
- 32xQSFP28 Ports

Data-Plane Programmability

- Intel Tofino Switch Silicon
- Barefoot Networks

Quad-Pipe Programmable Packet Processing Pipeline

6.4 Tbps Total Bandwidth

CPU: Intelx86 Xeon 2.0GHz

8-core/48GB/2TB SSD

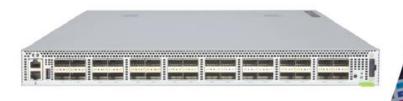




TOFINO 3<sup>™</sup>
25.6 Tbps
64x400 GE ports



TOFINO 1 <sup>™</sup> 6.4 Tbps



## **P4 Programmable Switches**





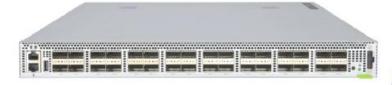
TOFINO 1 <sup>™</sup> 6.4 Tbps



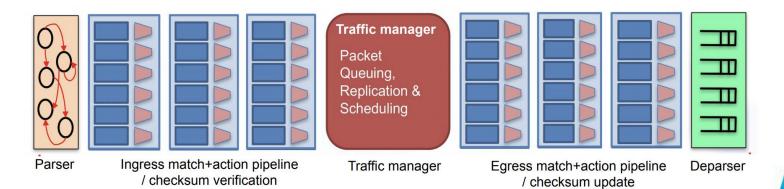
TOFINO 2<sup>™</sup> 12.8 Tbps 32x400 GE ports



TOFINO 3<sup>™</sup> 25.6 Tbps 64x400 GE ports



#### Portable Service Architecture (PSA) model



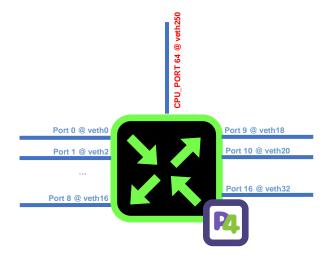


Slide courtesy P4.org

## RARE P4 program (aka bf\_router.p4) demo

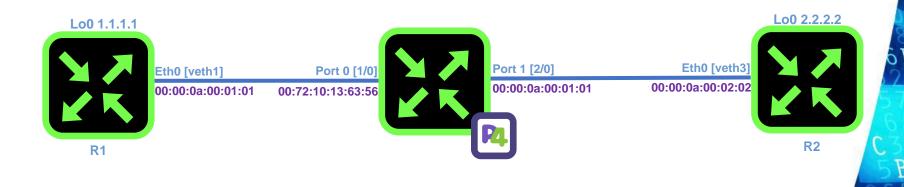


### bf\_switchd target virtual model



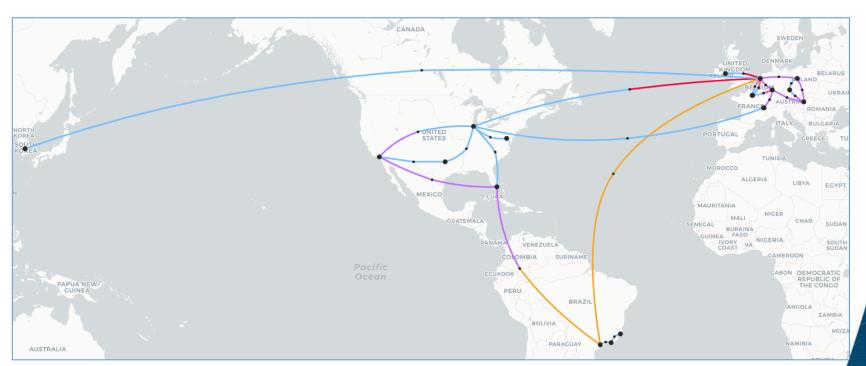


### RARE bf\_router.p4





#### **GP4L November 2022 during SC22!**



Develop & test your P4 program with GP4L!



## **PolKA - Polynomial Key-based Architecture for Source Routing** in **Network Fabrics**

- GP4L has been used to validate a <u>Research Paper</u> describing a innovative source routing paradigm: <u>Polka</u>
- After successful publication of Polka paper, it has been decided to implement this routing paradigm to RARE/FreeRtr routing stack

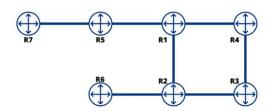


Figure 3. Edge-Core Experiment

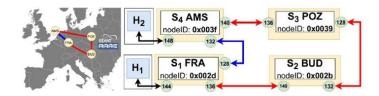


Figure 4. RARE/GEANT testbed

**Figure source**: https://sol.sbc.org.br/index.php/wpeif/article/download/21490/21314/by Federal Institute of Education Science and Technology of Espírito Santo, and Federal University of Espírito Santo, Espírito Santo, Brazil



#### **Looking ahead**



# Validate your use case with GP4L!

#### **Orchestrate and automate GP4L:**

Lab reservation

Persistent testbed interaction at global scale

#### **New hardware:**

TOFINO2, NVIDIA DPU, P4 SmartNIC, TOFINO/FPGA

#### **Global worldwide footprint:**

Interconnection with other persistent testbed

#### ? New idea:

Validate new use cases Focus on use case scalability 100/400 GE DTN automation Control plane scalability

And more ...



#### **Key take-away**

## You are welcome to work with us!

- freeRtr is the most feature rich Open Source control plane
- It has **multiple** dataplanes
- RARE/freeRtr API can be used to « hook » new dataplanes
- RARE dataplane can be automated by your control-plane
- Advanced features are enabled with specialised hardware (FPGA/NIC/DPU/ASIC) at control-plane level or dataplane level















#### **Useful Links**

**Documentation:** 

**GP4L project:** <a href="https://wiki.geant.org/display/GP4L/">https://wiki.geant.org/display/GP4L/</a>

**RARE/FreeRtr:** <a href="https://wiki.geant.org/display/RARE">https://wiki.geant.org/display/RARE</a>

https://blog.freertr.org

https://docs.freertr.org

https://blog.freertr.org

**GÉANT NETDEV**: <a href="https://wiki.geant.org/display/NETDEV">https://wiki.geant.org/display/NETDEV</a>

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## Thank you

Any questions?

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© GÉANT Association on behalf of the GN4 Phase 3 project

The research leading to these results has received funding

the European Union's Horizon 2020 research and innovation programme under Grant Agreement No. 856726 (GN4-3).